Using the HI3026 and HI3026A Evaluation Boards

Application Note | May 1999 | AN9652

Introduction

The purpose of this application note is to describe the evaluation boards for either the HI3026 or HI3026A 8-bit ultra high speed analog to digital converters (ADC). The main difference between the two devices is the maximum conversion speed of 120 MSPS and 140 MSPS respectively. This document will use HI3026 for both devices. The boards are shipped with the device soldered onto the PCB. The evaluation board includes many discrete components along with op amps, buffers, logic level conversion (ECL to TTL and TTL to ECL) and a 10-bit D/A converter for reconstructing the output of the HI3026. After latching the HI3026, input data with a frequency divided clock, the analog signal can be regenerated by a 10-bit high speed D/A converter. The latched data can also be extracted externally via a 24 pin cable connector.

Board Description

The evaluation platform is a two layer board optimized for high frequency operation. The supplies to the board should be low noise clean regulated linear power supplies. To ensure reliable performance, use the recommended operating conditions and never exceed the absolute maximum ratings shown in Table 1 and Table 2.

The signals in and out of the board are defined in the Pin Description table, which details various connectors and their function.

TABLE 1. OPERATING CONDITIONS

	MIN (V)	TYP (V)	MAX (V)
SUPPLY VOLTAGE			
V_{CC}	4.75	5.0	5.25
GND	-	0	-
V_{EE}	-5.50	-5.0	-4.75
+Amp	+3	+5	+7
-Amp	-7	-5	-3
|(+AMP)-(-AMP)|	9	10	11
ANALOG INPUT			
AMP.IN	-0.75	0	1.05
DIR.IN (V_{P-P})	1.5	2.0	2.2
CLOCK INPUT			
CLK.IN (V_{P-P})	0.75	0	1.05

TABLE 2. ABSOLUTE MAXIMUM RATINGS

	MIN (V)	MAX (V)
SUPPLY VOLTAGE		
V_{CC}	-0.5	7.0
V_{EE}	-7.0	0.5
+Amp	-0.5	7.0
-Amp	-7	0.5

Typical Performance Curves (HI3026A)

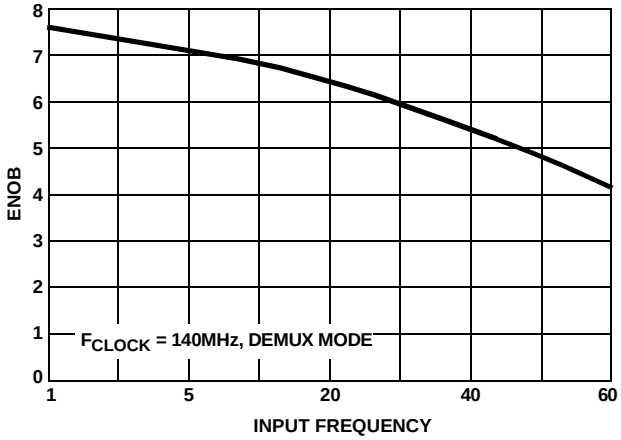


FIGURE 1. ENOB vs F_{IN}

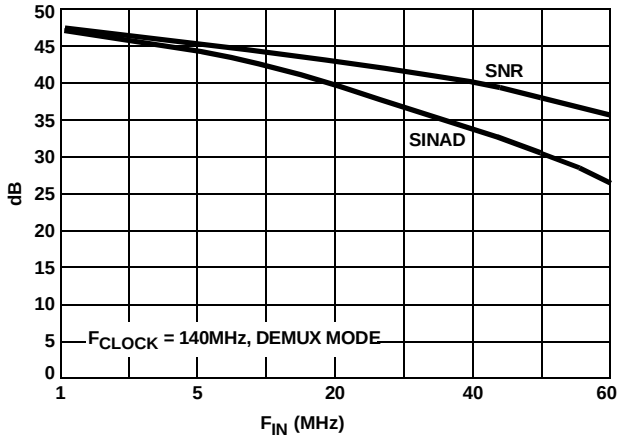


FIGURE 2. SINAD AND SNR

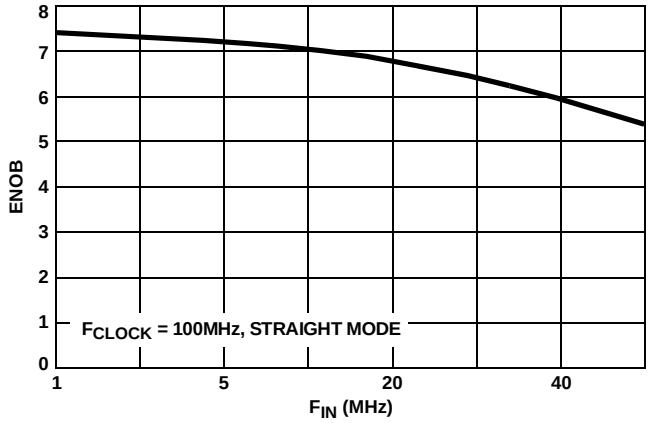


FIGURE 3. ENOB vs F_{IN}

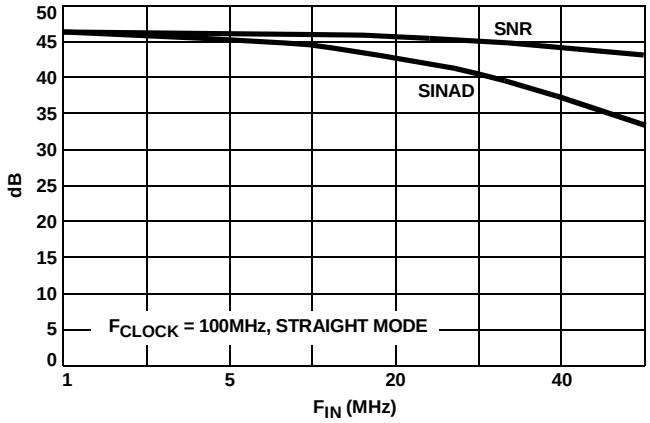


FIGURE 4. SINAD AND SNR

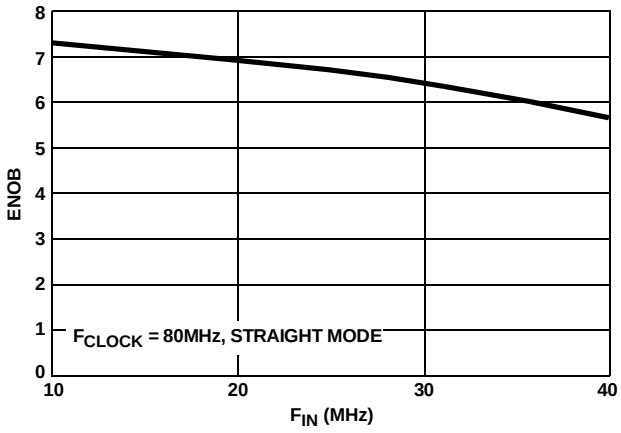


FIGURE 5. ENOB vs F_{IN}

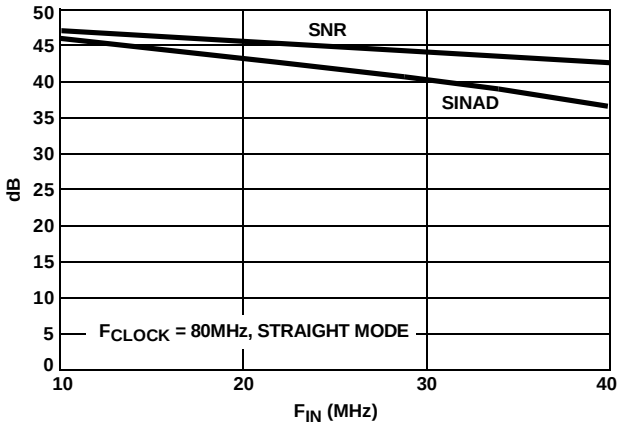
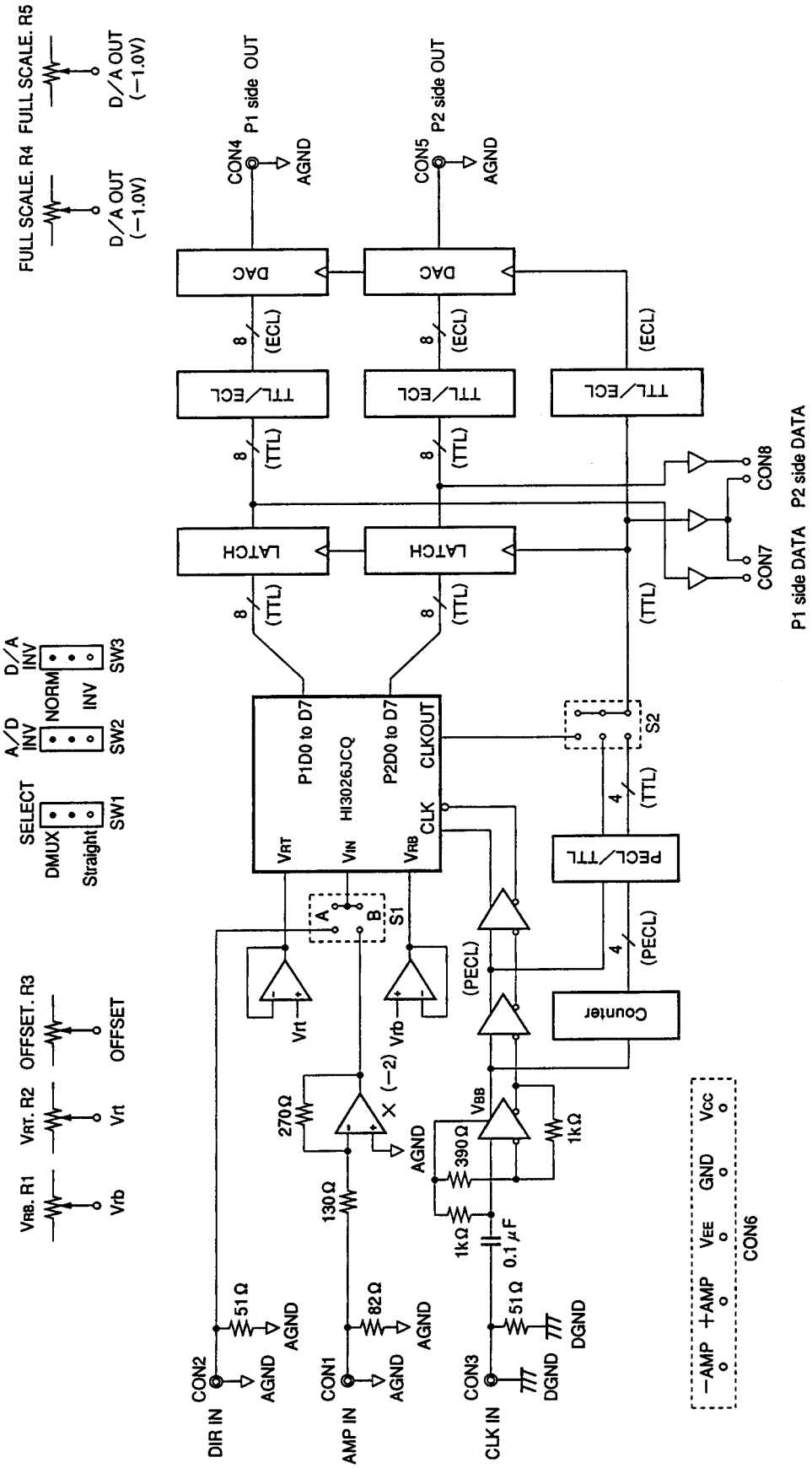


FIGURE 6. SINAD AND SNR

Pin Descriptions

PIN NO.	SYMBOL	I/O	STANDARD I/O LEVEL	CURRENT	DESCRIPTION
CON1	AMP.IN	I	0.95Vp-p		Doubles the analog input signal amplitude using the operational amplifier. The input impedance is 50Ω.
CON2	DIR.IN	I	2.0Vp-p		AC coupling input. suitable for sine waves and other repeating waveforms. The input impedance is 50Ω.
CON3	CLK.IN	I	1.0Vp-0		The HI3026 operates at the PECL level clock using the sine wave-to-PECL conversion circuit. The input impedance is 50Ω.
CON4	P1 Side OUT	O	0 to -1V		Allows the D/A converted waveform of the HI3026, port 1 side data to be observed. The output impedance is 50Ω.
CON5	P2 Side OUT	O	0 to -1V		Allows the D/A converted waveform of the HI3026, port 2 side data to be observed. The output impedance is 50Ω.
	V_{CC}	I	5.0V	0.8A	The inside of the board is divided into analog and digital systems.
	GND	I	0V		
	V_{EE}	I	-5.0V	-0.6A	
	+AMP	I	5.0V	40mA	+ side power supply for the operation amplifier.
	-AMP	I	-5.0V	-40mA	- side power supply for the operation amplifier.
CON7	P1 side DATA	O	TTL		The HI3026, port 1 side data output is latched at the frequency divided clock and then output.
CON8	P2 side DATA	O	TTL		The HI3026, port side data output is latched at the frequency divided clock and then output.

Block Diagram



Board Adjustments and Settings

1. VRB.R1: HI3026, VRB voltage adjusting volume.
2. VRT.R2: HI3026, VRT voltage adjusting volume.
3. OFFSET.R3: Adjusting volume for matching the AMP.IN input and DIR.IN input signal ranges to the HI3026, input range.
4. FULL SCALE.R4: Full-scale adjusting volume for the port 1 D/A output. (-1V: Typ.)
5. FULL SCALE.R5: Full-scale adjusting volume for the port 2 D/A output. (-1V: Typ.)
6. S1: Switching junction for the dual analog input pins.

   Set as follows according to the input pins used.

JUNCTION / SYMBOL	A	B
AMP.IN	OPEN	SHORT
DIR.IN	0.1µF	10kΩ

7. S2: Setting junction for the clock frequency division ratio. The operating speed after latching is determined by the frequency division ratio set here.

   When set to CLK OUT, it operates according to the HI3026, clock output.
8. SW1 SELECT: HI3026, output mode selector switch.
9. SW2 A/D INV: HI3026, output polarity inversion switch.
10. SW# D/A INV: D/A converter output polarity inversion switch.

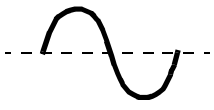
Notes on Board Operation

1. The factory settings for the HI3026, Evaluation Board are as follows:

VRB.R1 = 1.5V	FULL SCALE.R4 = -1V	S1 A···OPEN, B ···SHORT
VRT.R2 = 3.0V	FULL SCALE.R5 = -1V	S2 8···SHORT (1/8 frequency division)
OFFSET.R3 = 2.25V		

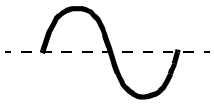
   When using the board in this condition, the input signals should be input at the amplitudes shown below. (The frequency is set as desired.)
2. When the analog signal is input from the CON1 (AMP.IN) pin, IC2:CLC404 limits the input dynamic range of the A/D converter's analog input signal according to the +AMP and -AMP supply voltages. The power supply for the operational amplifier can also be shifted to +AMP = +7.0V and -AMP = -3.0V to allow use with a wider input dynamic range.
3. When the analog input signal is a sine wave or other repeating waveform, the signal can be input form the CON2 (DIR.IN) pin with AC coupling. In these cases, the input dynamic range is not limited by the +AMP and -AMP supply voltages, but the VRT level may be limited by IC3:NJM3403A. Therefore, the power supply for the operational amplifier should be shifted in the same manner as in 2. above.
4. In the evaluation board of the HI3026, CLC404 (Comlinear) is employed for IC2 to drive the analog input signal. Though, CLC505 (Comlinear) can also be used instead of CLC404, there should be little change in the peripheral circuit in this case.

ANALOG INPUT SIGNAL: CON1 (AMP.IN)



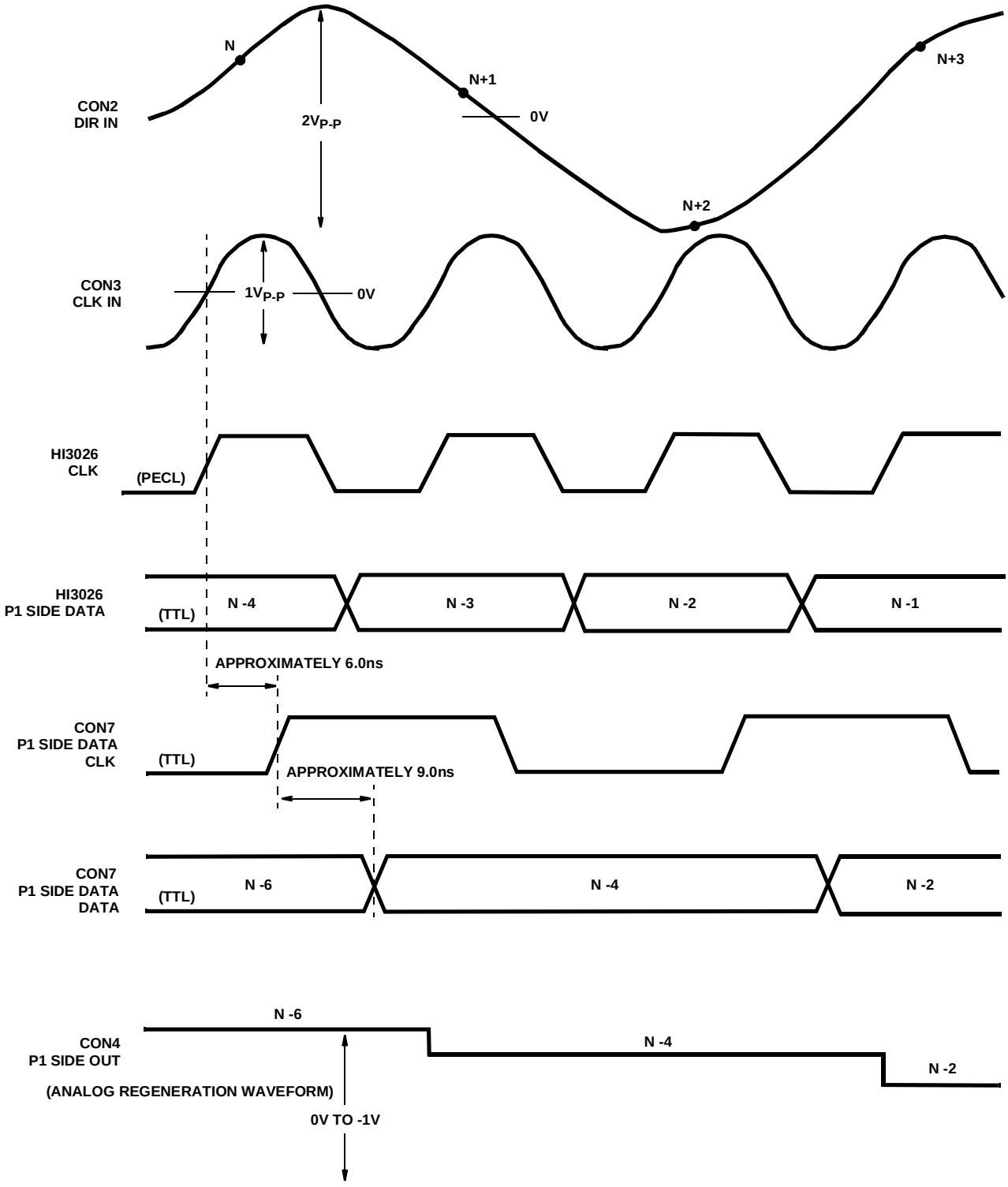
0V CENTER, 800mV$_{P-P}$ OR LESS

CLOCK INPUT SIGNAL: CON3 (CLK.IN)



0V CENTER, 1.0V$_{P-P}$

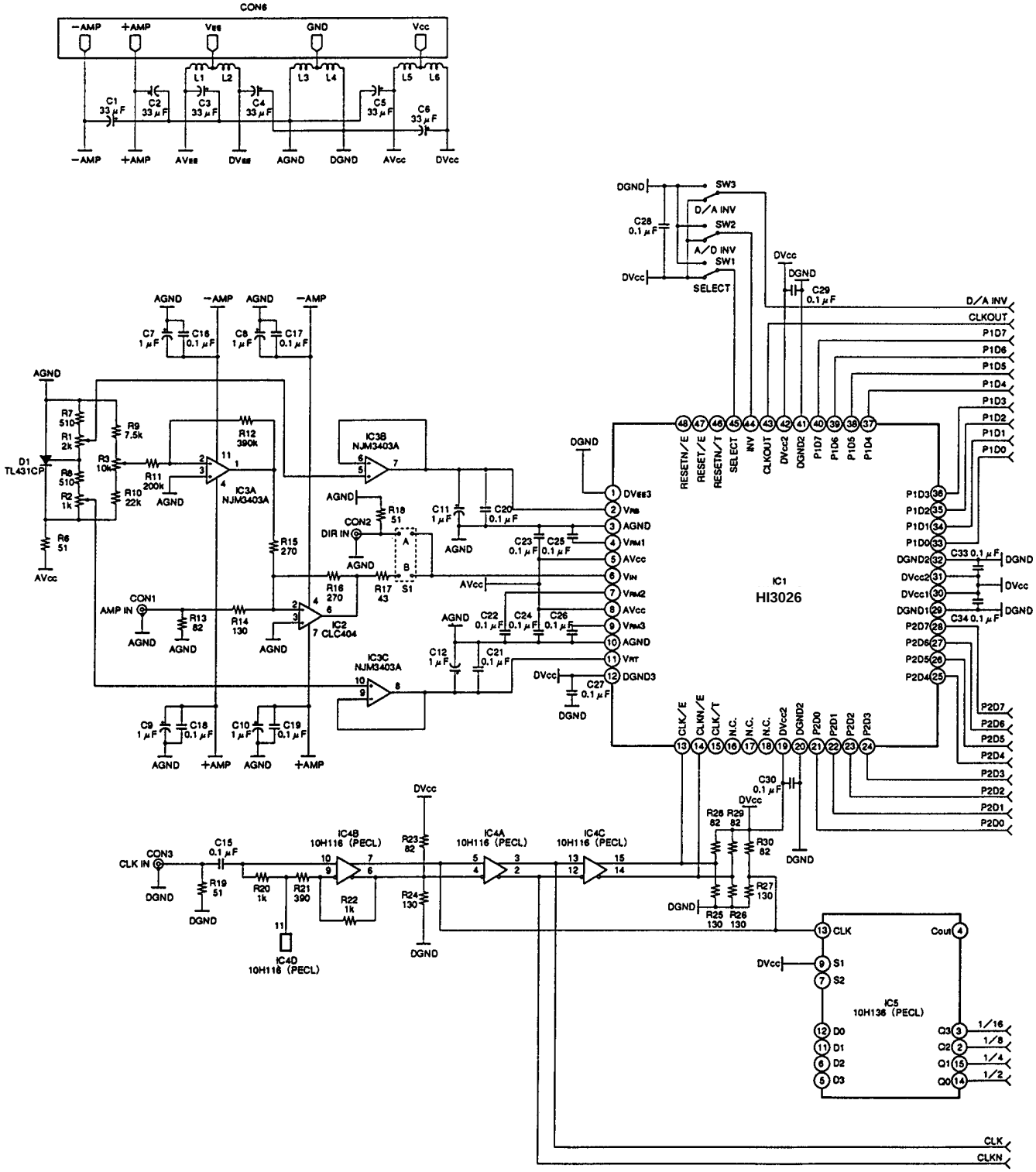
Timing Diagram



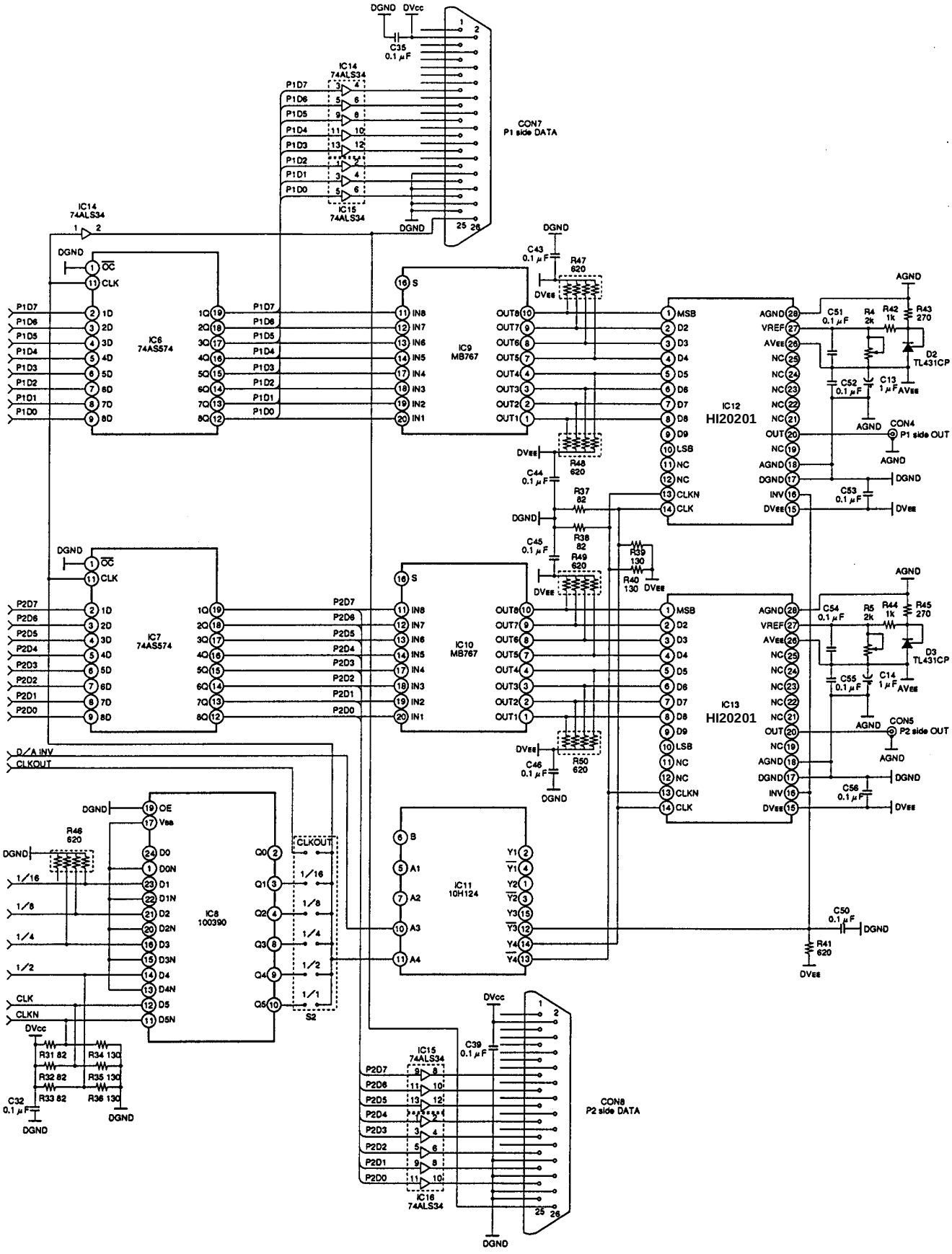
OPERATING CONDITIONS

HI3026 OPERATING MODE : STRAIGHT MODE
ANALOG INPUT : DIR IN PIN INPUT
S2 SETTING : 1/2 FREQUENCY DIVIDED CLOCK

Schematic Diagram



Schematic Diagram (Continued)



Component List

NO.	PRODUCT NAME	FUNCTION	NO.	PRODUCT NAME	FUNCTION
IC1	HI3026	8-bit A/D converter	R2	RJ-5W-1K	1kΩ volume resistor
IC2	CLC404AJE	OP-AMP	R1, 4, 5	RJ-5W-2K	2kΩ volume resistor
IC3	NJM3403AM	OP-AMP	R3	RJ-5W-10K	10kΩ volume resistor
IC4	MC10H116L	ECL buffer	R46 to 50	RGLD4X621J	620Ω network resistor
IC5	MC10H136L	ECL Countor			
IC6, 7	74AS574N	TTL Latch	R6, 18, 19	FRD-25SR (0.25W)	51Ω
IC8	100390	PECL→TTL conversion	R7, 8	FRD-25SR (0.25W)	510Ω
IC9, 10	MB767P	TTL→ECL conversion	R9	FRD-25SR (0.25W)-	7.5kΩ
IC11	MC10H124L	TTL→ECL conversion	R10	FRD-25SR (0.25W)	22kΩ
IC12, 13	HI20201JCB	10-bit D/A converter	R11	FRD-25SR (0.25W)	200kΩ
IC14 to 16	74ALS34	TTL Buffer	R12	FRD-25SR (0.25W)	390kΩ
D1 to 3	TL431CP	Shunt regulator	R13, 23 28 to 33, 37, 38	FRD-25SR (0.25W)	82Ω
SW1 to 3	ATE1D-2F3-10	Toggle switch	R14, 24 to 27, 34 to 36, 39, 40	FRD-25SR (0.25W)	130Ω
S1, 2	JX-1	Short pin	R15, 16, 43, 45	FRD-25SR (0.25W	270Ω
CON1 to 5	01K0315	BNC connector	R17	FRD-25SR (0.25W	43Ω
CON6	TJ-563	Power supply connector	R20, 22, 42, 44	FRD-25SR (0.25W	1kΩ
CON7, 8	(FAP-2601-1202)	Flat cable connector	R21	FRD-25SR (0.25W	390Ω
L1 to 6	ZBF503D-00	Fernite-bead filter	R41	FRD-25SR (0.25W	620Ω
C1 to 6	Tantal capacitor	33µF			
C7 to 12	Tantal capacitor	1µF			
C15	Ceramic capacitor	0.1µF			
All parts other than those listed above					
	Chip capacitor	0.1µF			

NOTE: CON7 and 8 are not mounted when boards are shipped. (Manufacturer: YAMAICHI Electronics Co., Ltd.)

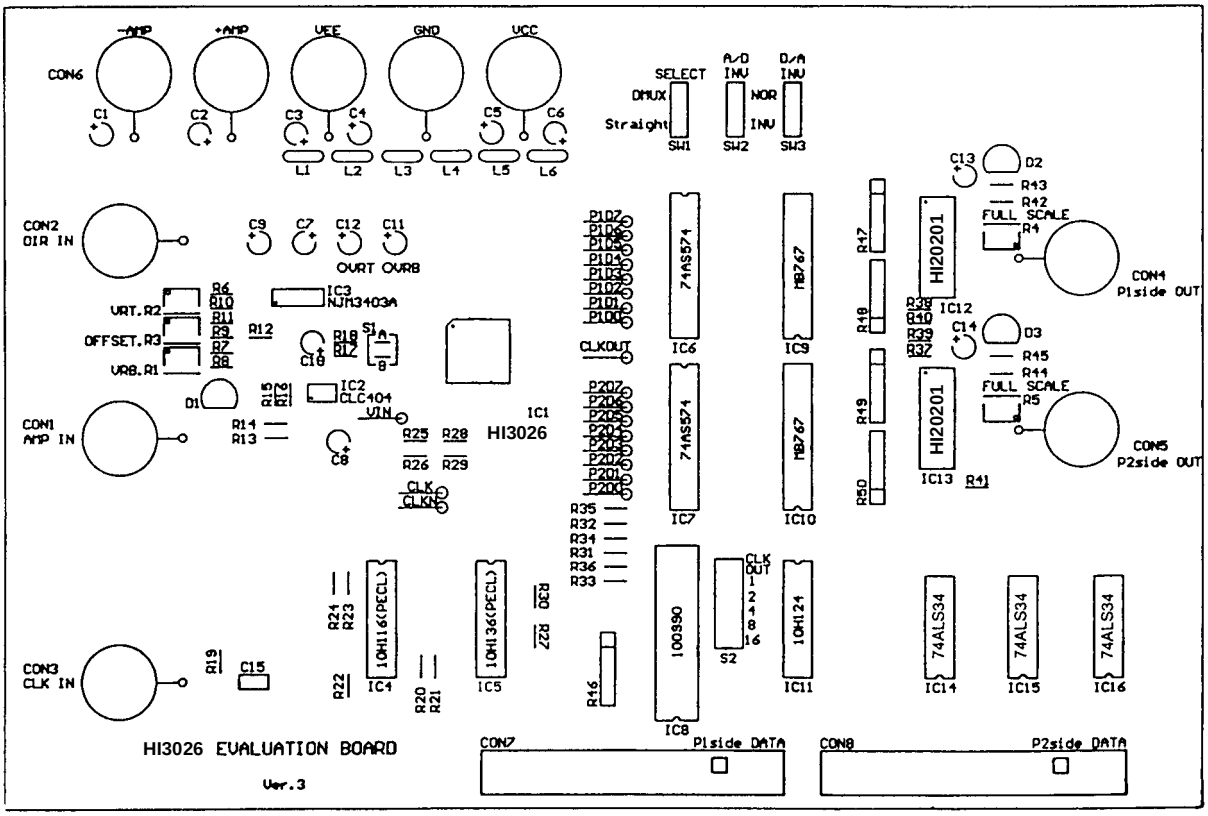


FIGURE 7. COMPONENT SIDE SILK DIAGRAM

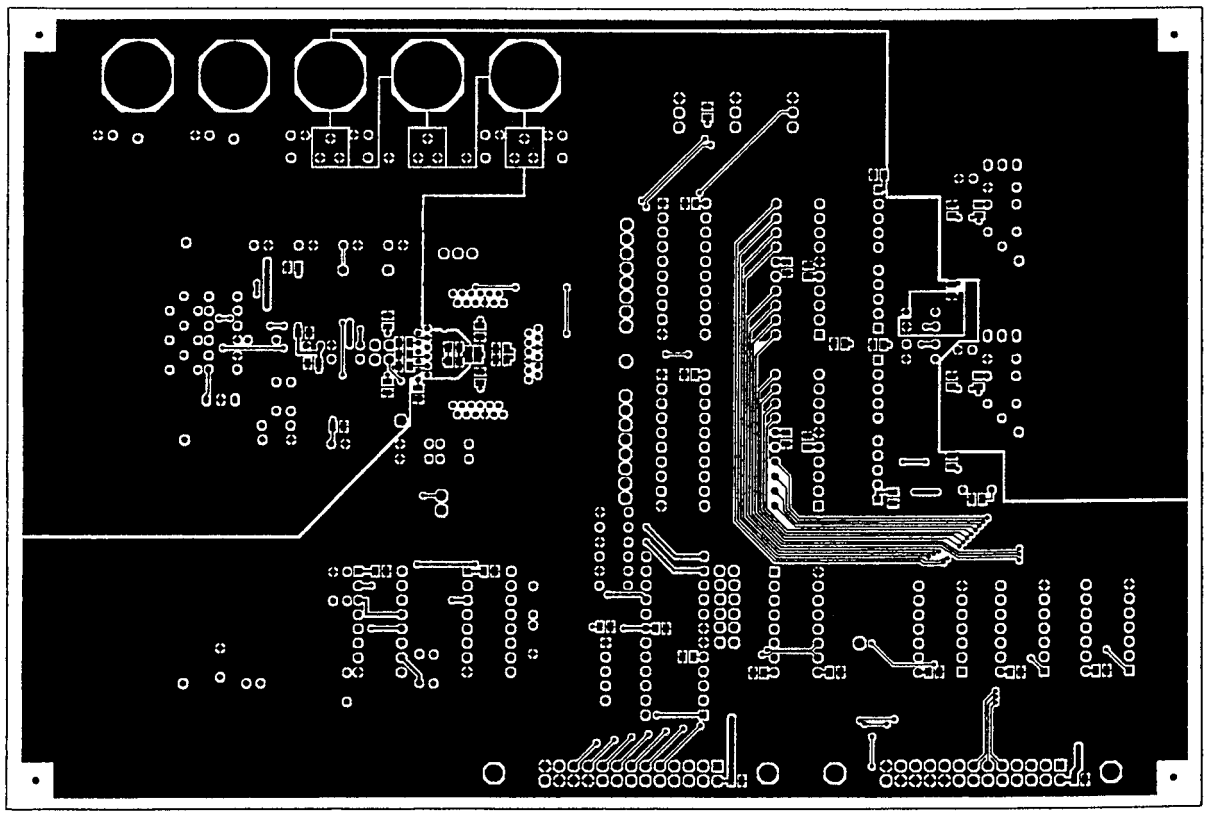


FIGURE 9. SOLDER SIDE SILK DIAGRAM

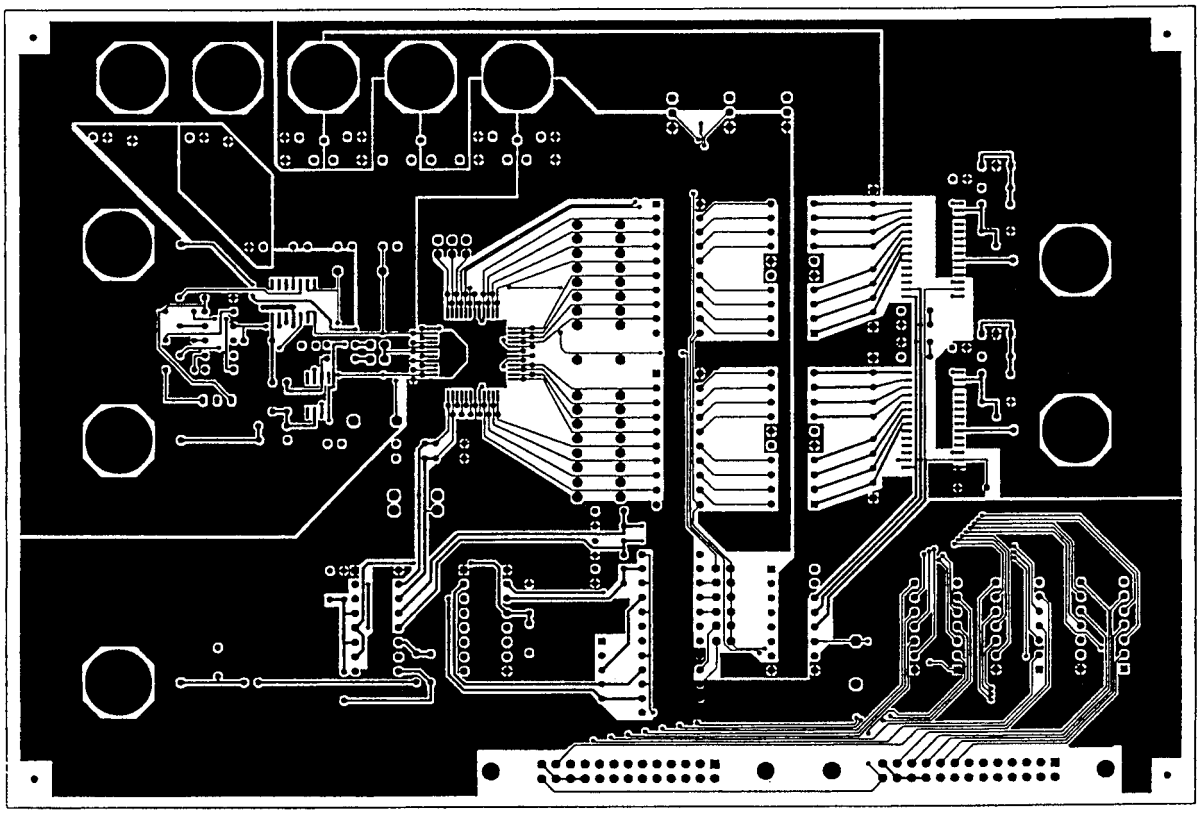


FIGURE 8. COMPONENT SIDE PATTERN DIAGRAM

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